REMARKS

Claims 1-30 are pending in the application. No claims are presently allowed.

Claims 1, 11, and 21 are amended to recite a processor capable of simultaneous execution of two or more threads of instructions. Support for this amendment is found at page 8, lines 5-6.

Claims 1, 11, and 21 are amended to recite that the resource unit is capable of being assigned to two or more of the threads. Support for this amendment is found at page 7, lines 25-28.

Claims 1, 11, and 21 are amended to clarify that the resource unit is assigned to the requesting thread. Support for this amendment is found at page 13, lines 21-24.

Claims 1, 5-11, 15-21, and 25-30 are amended to remove the variable "P" and replace it with "a," "the," "each," or nothing.

Claims 2, 12, and 22 are amended to cancel "instruction buffer unit."

Docket Number

Please change the docket number of this application to NC 84,779.

Claim Rejections – 35 U.S.C. § 102

Claims 1-30 have rejected under 35 U.S.C § 102(e) as allegedly anticipated by Blelloch et al. (UP 6,434,590).

Claim 1, as amended, is to a processor capable of simultaneous execution of two or more threads of instructions. The processor comprises at least one resource unit, a priority register, and a priority selector. The resource unit is capable of being assigned to two or more of the threads. The priority register stores thread information for the threads including a priority code corresponding to each thread. The priority selector generates an assignment signal to assign the resource unit to the requesting thread according to the priority codes.

Blelloch discloses a system and method of parallel processing. An assignment manager assigns tasks to a system of processing elements. Each processing element has a computation element CE and a memory element ME. Each computation element can access each memory element (col. 3, lines 9-18).

In order to make a *prima facie* case of anticipation, the reference must disclose each limitation of the claim. Blelloch does not disclose the limitation that the processor is capable of

simultaneous execution of two or more threads of instructions. In the present invention, a single processor (processing slice) can execute multiple threads. Although the specification discloses that multiple processing slices may be incorporated into multi-thread processor, each processing slice is capable of multi-thread processing on its own. However, Blelloch discloses a collection of processing elements, each one capable of only single-thread processing, as well as a separate assignment manager. Each performs only a single task at a time.

Blelloch also does not disclose the limitation that the thread requests the use of the resource unit. The thread is a series of instructions, some of which require the use of a resource. When such an instruction is encountered, a resource is requested. The request is triggered by the thread.

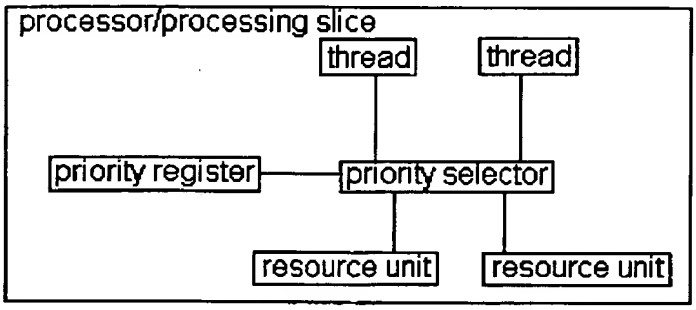
The Examiner stated that the processing element of Blelloch corresponds to the resource unit of the present claim. However, the resource unit is part of the processor, not the entire processor itself. Even if the processing element were a resource unit, the request to use the processing element is triggered by the assignment manager of Blelloch and not by the thread or task. The assignment of tasks to processing elements is based on time or memory (col. 3, lines 26-31), not based on the requirements of the operations to be performed by the task.

Blelloch also does not disclose the limitation that the resource unit is capable of being assigned to two or more of the threads. Resource units are parts of the processor that are used in executing instructions. Presently claimed examples are an instruction fetch unit, an instruction decoder and dispatcher, a memory access unit, a memory locking unit, a load unit, a store unit, a peripheral unit interface, an input/output unit, a functional unit, an arithmetic unit, a logic unit, and an arithmetic and logic unit. The resource unit is not a memory unit.

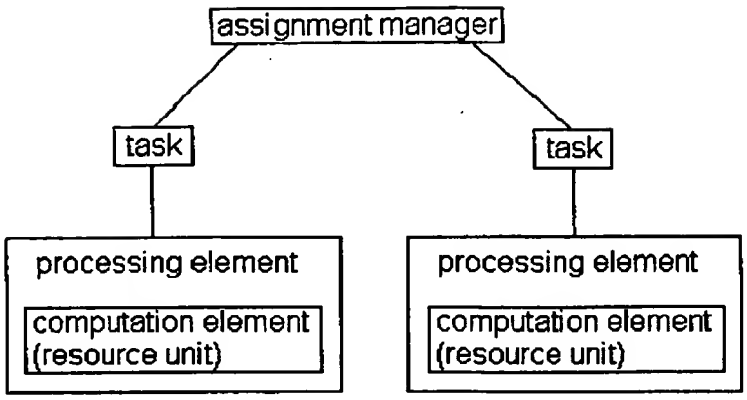
In the present invention, the processor has a resource unit that can perform operations from two or more and possibly each of the plurality of simultaneously executing threads. The processor is able to dispatch an instruction from any currently executing thread to any of such resource units within the processor. Thus, a resource unit within a given processor is shared among multiple threads that are simultaneously executing in that processor. This is an efficient design in that fewer resource units are needed. It is unlikely that all currently executing threads would need constant use of the resource units. Since each thread can use any resource unit, there can be full or near full utilization of resource units with little to no delay to wait for a resource unit to be available.

Blelloch discloses that each processing element has computation elements and memory elements, and that each computation element can read and write to each memory element. However there is no disclosure of a similar sharing of computation elements among the processing elements. A processing element cannot send a task to a computation element in a different processing element, which would be a more complex operation than merely using other memories. The result of this configuration is that the computation elements of any given processing element are dedicated only to the one thread that can execute on that processing element at a time. An idle computation element cannot be allocated to a thread executing on another processing element. In the present application, it is specifically recited in the claims that the resource unit can be assigned to *two or more* of the threads, which are simultaneously executing. Blelloch lacks this capability because any computation element within a processing element can be assigned to only *one* thread. The following diagrams schematically illustrate this difference.

Present Invention



Blelloch




Claims 11 and 21 are method and processor claims containing the limitations of claim 1, and claims 2-10, 12-20, and 22-30 depend from and contain the limitations of claims 1, 11, and 21, respectively. These claims are asserted to distinguish from the reference in the same manner as claim 1.

In view of the foregoing, it is submitted that the application is now in condition for allowance.

In the event that a fee is required, please charge the fee to Deposit Account No. 50-0281, and in the event that there is a credit due, please credit Deposit Account No. 50-0281.

Respectfully submitted,

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